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UTILITY APPLICATION FOR UNITED STATES PATENT  
FOR  
POWER-UP CIRCUIT IN SEMI-CONDUCTOR MEMORY DEVICE

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POWER-UP CIRCUIT IN SEMICONDUCTOR MEMORY DEVICE

Field of the Invention

5        The present invention relates to a semiconductor memory device; and, more particularly, to a power-up circuit in a semiconductor memory device.

Description of Related Art

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Generally, a semiconductor memory device includes various internal logics and an internal voltage generation circuit for securing stable element operation. The operations of the logics should be initialized to specific states before a 15 normal operation. Also, the internal voltage generating circuit provides a bias voltage to the internal logics of the semiconductor memory device. If the bias voltage does not have a desired voltage level when a power supply voltage VDD is applied from an external circuit, some problems such a 20 latch-up are caused. Therefore, it is difficult to obtain reliability of the semiconductor memory device. In order to solve the latch-up due to instabilities of the internal voltage and the initialization of the internal logics, the semiconductor memory device has a power-up circuit.

25        The power-up circuit is not operated in response to a voltage level of the power supply voltage VDD as soon as the power supply voltage VDD is applied in an initialization

operation of the semiconductor memory device, but operated when the level of the power supply voltage VDD is increased to a critical voltage level.

A power-up signal outputted from the power-up circuit is 5 maintained to a logic low level until the level of the power supply voltage VDD is lower than the critical voltage level by sensing voltage increase of the power supply voltage VDD applied from an external circuit, and transited to a logic high level when the level of the power supply voltage level 10 VDD is stabilized to over the critical voltage level. In contrary, when the voltage level of the power supply voltage VDD is decreased, the power-up signal is maintained with a logic high level until the voltage level of the power supply voltage VDD is higher than the critical voltage level, and 15 then, when the voltage level of the power supply voltage VDD is decreased under the critical voltage level, the power-up signal is transited to a logic low level.

After the power supply voltage is applied, latches included in the internal logics of the semiconductor memory 20 device are initialized to predetermined values while the power-up signal is a logic low level, and an initialization operation of the internal voltage generation circuit is also carried out at this time.

Meanwhile, the critical voltage level of the power supply 25 voltage VDD, which the power-up signal is transited, is to perform normal switching operations of logics. The critical voltage level is designed to be a larger than that of the

threshold voltage of the MOS transistor. If the critical voltage level is designed to be the same level with the threshold voltage of the MOS transistor, there is no problem to initialize digital logics. However, in an internal power 5 circuit configured with an analog circuit, e.g., boosted voltage (VPP) generator, since an operation efficiency is decreased, a latch-up may be caused after a power-up trigger. Therefore, the critical voltage level is designed to be larger than the threshold voltage of the MOS transistor to stably 10 operate the analog circuit after the power-up trigger.

Fig. 1 is a circuit diagram showing a conventional power-up circuit in a semiconductor memory device.

As shown, the conventional power-up circuit includes a power voltage level follower unit 100, a power voltage trigger 15 unit 110 and a buffer unit 120.

The power voltage level follower unit 100 provides a bias voltage  $V_a$  which increases or decreases linearly in proportion to a power voltage  $VDD$ . The power voltage trigger unit 110 serves to detect that a voltage level of the power voltage  $VDD$  20 becomes a critical voltage level in response to the bias voltage  $V_a$ . The buffer unit 120 generates a power-up signal  $pwrup$  by buffering a detection bar signal  $detb$  outputted from the power voltage trigger unit 110.

Herein, the voltage level follower unit 100 is provided 25 with a first resistor  $R1$  and a second resistor  $R2$  connected between the power voltage  $VDD$  and a ground voltage  $VSS$  for a voltage division.

The power voltage trigger unit 110 includes a P-channel metal oxide semiconductor (PMOS) transistor MP0, an N-channel metal oxide semiconductor (NMOS) transistor MN0 and a first inverter INV0.

5 The PMOS transistor MP0 is connected between the power voltage VDD and a node N1 and its gate is connected to the ground voltage VSS. The NMOS transistor MN0 is connected between the ground voltage VSS and the node N1 and its gate is connected to the bias voltage Va. The first inverter INV0  
10 receives a detect signal det from the node N1 to output the detection bar signal detb. Herein, the PMOS transistor MP0 can be replaced with another load element having the same valid resistance as that of the PMOS transistor MP0.

15 Meanwhile, the buffering unit 120 is provided with a plurality of inverters INV1 to INV4 for receiving the detection bar signal debt to output the power-up signal pwrup.

Fig. 2 is a timing diagram showing an operation of the conventional power-up circuit shown in Fig. 1.

20 The bias voltage Va outputted from the power voltage level follower unit 100 is varied as a following equation 1:

$$Va = \frac{R2}{R1+R2} \times VDD \quad \text{Eq. 1}$$

25 That is, the bias voltage Va is increased as the voltage level of the power voltage VDD is increased. If the bias voltage Va is increased to be higher than a threshold voltage of the NMOS transistor MN0, the NMOS transistor MN0 is turned on and the detect signal det is changed depending on currents

flown on the PMOS transistor M<sub>P0</sub> and the NMOS transistor M<sub>N0</sub>.

At an initial state, the detection signal det is increased following the power voltage VDD. Thereafter, as the bias voltage Va is increased, the NMOS transistor M<sub>N0</sub> has an increased current flow and the detection signal det is changed to a logic low level at a predetermined voltage level of the power supply voltage VDD. At this time, when the voltage level of the detection signal det crosses a logic threshold value of the first inverter INV0, a voltage level of the detection bar signal detb is increased following the power supply voltage VDD. The detection bar signal detb outputted from the first inverter INV0 is buffered in the buffer unit 120 and outputted as the power-up signal pwrup having a logic high level.

However, after the power supply voltage is stabilized, a power drop can be occurred by a power noise, current consumption due to a temporary operation of the device, current consumption of a resistor or the like. In a trend that an operation voltage of the semiconductor memory device is decreased, since the conventional power-up circuit detects an abnormal falling of the voltage level, a reset operation abnormally operated by the power-up signal pwrup can not be prevented. Thereafter, even if the power up signal returns to a logic high level as the power-up signal pwrup is recovered to a previous voltage level, an abnormal reset may cause an unstable operation of a semiconductor memory device.

### Summary of the Invention

It is, therefore, an object of the present invention to provide a power-up circuit in a semiconductor memory device 5 capable of preventing an abnormal reset operation due to a power drop.

In accordance with an aspect of the present invention, there is provided a power-up circuit of a semiconductor memory device, including: a power supply voltage level follower unit 10 for providing a bias voltage which is linearly varied according to variation of a power supply voltage; a power supply voltage detection unit for detecting the variation of the power supply voltage to a predetermined critical voltage level in response to the bias voltage; and a reset prevention 15 unit for canceling variation of the detection signal due to a power drop by delaying level transition of the detection signal according to decrease of the power supply voltage.

### Brief Description of the Drawings

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The above and other objects and features of the instant invention will become apparent from the following description of preferred embodiments taken in conjunction with the accompanying drawings, in which:

25 Fig. 1 is a circuit diagram showing a conventional power-up circuit in a semiconductor memory device;

Fig. 2 is a timing diagram showing an operation of the

conventional power-up circuit shown in Fig. 1;

Fig. 3 is a circuit diagram illustrating a power-up circuit in accordance with the preferred embodiment of the present invention; and

5 Fig. 4 is a timing diagram showing an operation of the power-up circuit of Fig. 3 in accordance with the present invention.

#### Detailed Description of the Invention

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Hereinafter, a power-up circuit in a semiconductor memory device according to the present invention will be described in detail referring to the accompanying drawings.

15 Fig. 3 is a circuit diagram illustrating a power-up circuit in accordance with the preferred embodiment of the present invention.

As shown, the power-up circuit includes a power supply voltage level follower unit 200, a power supply voltage detection unit 210, a reset prevention unit 220 and a buffer unit 230. The power supply voltage level follower unit 200 provides a bias voltage  $V_a$ , which is linearly varied according to a voltage level of the power supply voltage VDD, by using the power supply voltage VDD and a ground voltage VSS. The power supply voltage detection unit 210 detects whether the power supply voltage VDD is transited to a predetermined critical voltage level in response to the bias voltage  $V_a$ . The reset prevention unit 220 cancels variation of a detection

signal, which is outputted from the power supply voltage detection unit 210, due to a power drop by delaying a transition of the detection signal to a logic low level. The buffer unit 230 outputs a power-up signal pwrup by buffering 5 an output signal detbn of the reset prevention unit 220.

The power supply voltage level follower unit 200 is provided between a power supply voltage VDDD and a ground voltage VSS and includes a first resistor and a second resistor R1 and R2. Also, the first and second resistors R1 10 and R2 can be configured with an active resistor such a MOS transistor.

The power supply voltage detection unit 210 includes a PMOS transistor MP0 whose gate is connected to the ground voltage VSS, an NMOS transistor MN0 whose gate receives the 15 bias voltage Va, and an inverter INV0. The PMOS transistor MP0 is connected between the power supply voltage VDD and a first node N1 and the the NMOS transistor MN0 is connected between the first node N1 and the ground voltage VSS. The inverter receives the detection signal det outputted from the 20 first node N1. Also, the PMOS transistor MP0 can be replace with another load element having the same effective resistance with that of the PMOS transistor MP0.

As described in the above, the power supply follower unit 200 and the power supply voltage detection unit 210 of the 25 power-up circuit in accordance with the present invention are identically configured with those of the power-up circuit illustrated in Fig. 1. Therefore, the reference numerals in

Fig. 3 are identically used for the same elements in Fig. 1.

The reset prevention unit 220 includes pull-up and pull-down transistors MP2 and MN2 whose gates receive an output signal debt of the power supply voltage detection unit 210, a 5 response delay unit 225 for delaying a pull-up operation of the pull-up PMOS transistor MP2 in response to transition of the output signal debt of the power supply voltage detection unit 210, and an inverter connected to the pull-up and pull-down transistors MP2 and MN2. The response delay unit 255 10 includes a delay 20 for delaying the output signal debt of the power supply voltage detection unit 210 as much as a predetermined time and a MPOS transistor MP1 which is connected between the power supply voltage VDD and the pull-up PMOS transistor MP2 and whose gate receives an output signal 15 of the delay 20. The delay 20 can be also replaced with a general delay element such as a resistor, capacitor or the like.

The buffer unit 230 is configured with an inverter chain constituted with two inverters INV6 and INV7. The buffer unit 20 230 receives an output signal detbn of the reset prevention unit 220.

Fig. 4 is a timing diagram showing an operation of the power-up circuit of Fig. 3 in accordance with the present invention.

25 As shown, a bias voltage Va level is increased as the power supply voltage VDD is increased after applying the power supply voltage VDD. If the bias voltage Va level is increased

to over a threshold voltage level of the NMOS transistor MN0 in the power supply detection unit 210, the NMOS transistor is turned on, so that a voltage level of the detection signal is varied according to current flows in the PMOS transistor,  
5 which acts as a load, and the NMOS transistor MN0.

Since the NMOS transistor MN0 is turned on at an initial stage, a voltage level of the detection signal det is increased according to increase of the power supply voltage VDD level. As the bias voltage Va level is increased, since a  
10 current drivability of the NMOS transistor is increased, the voltage level of the detection signal det is transited to a logic low level at a specific level of the power supply voltage level VDD. At this time, if the voltage level of the detection signal det becomes over a logic threshold level of  
15 the inverter INV0, the output signal debt of the inverter INV0 is increased according to the increase of the power supply voltage VDD.

When the output signal debt of the power supply voltage detection unit 210 becomes a logic high level, the pull-down  
20 NMOS transistor MN2 of the reset prevention unit 220 is turned on to thereby discharge a second node N2, and the output signal detbn of the inverter INV5 becomes a logic high level. Thereafter, the output signal detbn makes that a power-up signal pwrup is transited to a logic high level by being  
25 buffered in the buffer unit 230.

In the above procedure, an operation of the power-up circuit in accordance with the present invention is mostly

identical to that of the conventional power-up circuit in Fig. 1.

As described in the prior art, when the power drop is occurred, the power supply voltage detection unit 210 detects 5 the drop of the power supply voltage VDD level, so that the voltage level of the detection signal det is increased and the output signal debt of the inverter INV0 is pulsed to a logic low level. If the output signal debt of the INV0 is pulsed to a logic low level, the pull-up PMOS transistor MP2 is turned 10 on and the pull-down transistor MN2 is turned off.

However, the pull-up operation of the pull-up PMOS transistor MP2 can be performed only when the PMOS transistor MP1 of the response delay unit 225 is turned on. Since the PMOS transistor MP1 of the response delay unit 225 receives 15 not the output signal debt of the inverter INV0 but a delayed output signal detbd of the inverter INV0 as a gate input, the PMOS transistor MP1 is turned on after the predetermined delay 20 since the output signal detb of the inverter INV0 is pulsed to a logic low level.

If a delay time of the delay 20 is configured to have 20 longer time than a time that the output signal detb is maintained to a logic low level, the pull-up operation is not carried out by the PMOS transistors MP1 and MP2. Therefore, even if the power-up signal pwrup is temporarily decreased, 25 the power-up signal pwrup is not transited to a logic low level.

Accordingly, even though the power drop is occurred after

the power-up signal pwrup is transited to a logic high level, undesired initialization operations of internal logics can be prevented by the power-up circuit in accordance with the present invention. Therefore, malfunctions of the 5 semiconductor memory device due to the undesired initialization operation can be prevented.

In accordance with the preferred embodiment of the present invention, the reset prevention unit 220 is configured to a pull-up side. However, the response delay unit 225 can 10 be arrayed at a pull-down side according to a characteristic of the detection signal det.

While the present invention has been described with respect to the particular embodiments, it will be apparent to those skilled in the art that various changes and 15 modifications may be made without departing from the spirit and scope of the invention as defined in the following claims.